CLAIMS

Please amend the Claims as follows:

1. – 30. (Cancelled).

31. (New) A floating point unit (FPU), comprising:

an exponent logic (EL), comprising:

an exponent operand selection logic configured to receive a first exponent signal Ea, a second exponent signal Eb, and a third exponent signal Ec, and to generate first intermediate signal Ex, second intermediate signal Ey, and third intermediate signal Ez based on signals Ea, Eb, and Ec;

a 3:2 compressor configured to receive the signals Ex, Ey, and Ez, and to generate a carry signal and a sum signal based on the signals Ex, Ey, and Ez; and

a 3-way compound adder configured to receive the carry signal, the sum signal, and the signal Ez, and to generate a first EL output signal S0, a second EL output signal S1, and a third EL output signal S2 based on the received carry signal, sum signal and signal Ez;

wherein the signal S0 represents an exponent value "e", the signal S1 represent the exponent value "e+1", and the signal S2 represents the exponent value "e+2";

an exponent adjust and rounding logic (EAD) coupled to the EL and to a result generator, the EAD configured to receive the signals S0, S1, and S2, an inverted anticipated leading zero shift signal (!LZA), a corrected leading zero shift signal (LZA_CORR), and a special case signal, the EAD configured to:

generate a first output signal E2A based on the received S1 and !LZA signals;

generate a second output signal E2B based on the received S2 and !LZA signals;

generate a results select signal based on the received signals S0, S1, S2, !LZA, LZA_CORR and the special case signal; and

transmit the results select signal, and the signals E2A and E2B to the result generator.

32. (New) The FPU of Claim 31, wherein the EAD further comprises a first adder configured to receive the signals S1 and !LZA and to generate the first output signal E2A based on the received signals S1 and !LZA.

33. (New) The FPU of Claim 31, wherein the EAD further comprises a second adder configured to receive the signals S2 and !LZA and to generate the first output signal E2B based on the received signals S2 and !LZA.

34. (New) The FPU of Claim 31, wherein the EAD further comprises a result multiplexer configured to generate the results select signal based on the received signals S0, S1, S2, !LZA, LZA_CORR and the special case signal.

35. (New) The FPU of Claim 31, wherein the EAD is further configured to determine whether an underflow condition exists based on the signals S0 and !LZA.

36. (New) The FPU of Claim 31, wherein the EAD is further configured to determine whether an underflow condition exists based on the signals S1 and !LZA.

37. (New) The FPU of Claim 31, wherein the EAD further is further configured to determine whether an overflow condition exists based on a first most significant bit (MSB) and a second MSB of the signal E2B.

38. (New) The FPU of Claim 31, wherein the signals Ex and Ey represent 8-bit numbers and the signal Ez represents a 10-bit number.

39. (New) The FPU of Claim 38, wherein the a first most significant bit (MSB) and a second MSB of the signal Ez are input to the 3-way compound adder and bypass the 3:2 compressor.

40. (New) The FPU of Claim 31, wherein the EAD is further configured to check for exceptions substantially in parallel generation of the signals E2A and E2B.

41. (New) The FPU of Claim 31, wherein the signals S0, S1, S2 represent 10-bit 2's complement numbers, with a bias of 127.

42. (New) The FPU of Claim 31, wherein the FPU is configured to perform fast mode rounding.

43. (New) The FPU of Claim 42, wherein the FPU is further configured to perform fractional truncation.